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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/767,065
Filing Date: January 29, 2004
Appellant(s): FURUKAWA ET AL.

William Allen
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed October 4, 2010 appealing from the Office action mailed May 5, 2010.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application: Claims 1-6 and 8.

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

6,556,704	Choi et al.	5-2003

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al.

Regarding claim 1, Choi et al. teach in figure 3F and related text a vertical transistor device structure formed on a substrate 200, the substrate 200 defining a substantially horizontal plane, the transistor device structure comprising:

a source region 40;

a drain region 50;

a gate electrode 20 disposed on the substrate, said gate electrode positioned vertically between said source region and drain region; and

a nanotube 100 including a first end physically and electrically coupled with said source region, a second end electrically coupled with said drain region, and a channel region extending vertically through said gate electrode between said source region and said drain region, and

said gate electrode configured to receive a control voltage effective to regulate current flow through said channel region between said source region and said drain region.

Choi et al. do not explicitly state in the embodiment of figure 3F a plurality of semiconducting nanotubes.

Choi et al. teach using a plurality of semiconducting nanotubes in the disclosed invention of a nano sized transistor (see, for example, column 3, lines 39-43), wherein figures 1-3 depict only a unit cell of the transistor (column 3, lines 41-43).

Choi et al. further teach in the embodiment of figure 4B connecting the plurality of semiconducting nanotubes 100 with a single drain region 50 and a single source region 40.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a plurality of unit cells of the transistor in Choi et al.'s device, such that a plurality of semiconducting nanotubes are present in the device, and to connect the plurality of semiconducting nanotubes with a single drain region and a single source region, in order to use the device in a practical application which requires a plurality of semiconducting nanotubes, such as a nano sized transistor, and in order to simplify the processing steps of making the device and to simplify the operation of the device, respectively.

Regarding claims 4-6 and 8, Choi et al. teach in figure 1 and related text an insulating layer 30 disposed between said drain and said gate electrode for electrically isolating said drain from said gate electrode, an insulating layer 10 disposed between said source and said gate electrode for electrically isolating said source from said gate electrode, wherein said at least one semiconducting nanotube is composed of arranged carbon atoms, wherein said at least one semiconducting nanotube is oriented substantially perpendicular to said horizontal plane.

Regarding claims 2-3, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the source and drain of a catalyst material effective for growing said at least one semiconducting nanotube in Choi et al.'s device in order to simplify the processing steps of making the device.

Note that the process limitations of forming the source and drain of a catalyst material effective for growing said at least one semiconducting nanotube, would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. A “product by process” claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a “product by process” claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in “product by process” claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

(10) Response to Argument

1. Appellants argue on pages 4 and 5 that the examiner’s statement that the claimed limitation of “electrically coupled”, as recited in claim 1, should not have the same limitation as “physically connected” is ”unreasonable”.

Appellants further argue that *“In distinguishing "electrical coupling" from "physical coupling", the Examiner recognizes that each nanotube in Figures 1-3 of Choi and each nanotube in Figure 4B of Choi is not "physically coupled" with the same source and drain region as any other nanotube. However,*

the Examiner is improperly construing the term "electrical coupling" so broadly as to admit to a meaning that entirely eliminates any path for current flow".

1. The examiner strongly objects to appellants' statement that the examiner "recognizes" or "admits" that Choi et al. do not teach the limitation "physically coupled". To clarify the record, the examiner never "recognized" and never "admitted" that Choi et al. do not teach the limitation "physically coupled". On page 8 of the May 5, 2010 office action, the examiner merely made a distinction between the claimed limitation of "electrically coupled" and the phrase "physically connected".

The fact is that claim 1 recites "electrically coupled". Claim 1 does not recite "physically connected". It is well known that the phrase "electrically coupled" is not synonymous to the phrase "physically connected". In fact, it is well known in the art that the limitation brought by the phrase "electrically coupled" is much broader than the limitation brought by the phrase "physically connected". If a claim recites that two elements are "electrically coupled", then the two elements are only required to have some electrical coupling there-between. The two elements are not required to be directed connected with each other. If, on the other hand, a claim recites that two elements are "physically connected", then the two elements must be in direct contact with each other. The Board is respectfully urged to re-affirm the position that a limitation brought by the phrase "electrically coupled" is not synonymous, and in fact broader than the limitation brought by the phrase "physically connected".

Regarding the Choi et al. reference, although the limitation of "physically coupled" is taught by Choi et al. (please see discussion below), said limitation is not

required by the broad recitation of the claim, which merely calls for "electrically coupled".

2. Appellants argue in the passage bridging pages 5 and 6 that *"a person having ordinary skill in the art would not conclude the device structure in Figure 4B includes plural nanotubes that are electrically coupled with the same source and drain regions".*

2. Claims 1-6 and 8 are rejected over the embodiment of figures 1-3 of Choi et al., and not over the embodiment of figure 4B. Although the rejection of claims 1-6 and 8 is not based on the embodiment of figure 4B, the examiner disagrees that the structure depicted in figure 4B includes plural nanotubes that are not electrically coupled with the same source and drain regions. The embodiment of figures 4A and 4B describes a vertical nano-sized transistor (column 4, lines 33-38). The circuit diagram of the transistor of figure 4B is depicted in figure 4A. It is clear from figure 4A that plurality of nanotubes 100 are electrically coupled and physically connected between one source region 40 and one drain region 50. Furthermore, even without the consideration of the circuit diagram of figure 4A, figure 4B depicts one device comprising plurality of nanotubes 100, four source regions 40 and two drain regions 50. Since all the elements of said transistor are electrically coupled to each other, then the plurality of nanotubes 100 are electrically coupled between one source region 40 and one drain region 50.

3. Appellants argue on page 6 that it would not have been objectively reasonable to a person having ordinary skill in the art to change the embodiment of the device structure in Figures 1-3 of Choi by adding plural nanotubes, in order to use the device in a practical application which requires a plurality of semiconducting nanotubes.

Appellants further argue in the second paragraph on page 7 that *"replacing a single nanotube (100) extending between the source (40) and drain (50) in the structure of Figures 1-3 with multiple nanotubes extending between the source (40) and drain (50)"* will not simplify the processing steps of making the device and will not simplify the operation of the device.

Appellants continues to argue on page 7 that *"the generalizations regarding the plural term "carbon nanotubes" made at column 3, lines 39-43 of Choi fail to support the Examiner's conclusion that the unit cell shown in Figures 1-3 of Choi can be modified to include more than one semiconducting nanotube".*

3. The rejection of claims 1-6 and 8 over Choi et al. **is not** based on changing the unit cell depicted in figures 1-3 by replacing the single nanotube 100 extending between the source 40 and drain 50 with multiple nanotubes extending between the source and drain regions, as argued by appellants.

The rejection of claim 1 recites:

"Choi et al. do not explicitly state in the embodiment of figure 3F a plurality of semiconducting nanotubes. Choi et al. teach using a plurality of semiconducting nanotubes in the disclosed invention of a nano sized transistor (see, for example, column 3, lines 39-43), wherein figures 1-3 depict only a unit cell of the transistor (column 3, lines 41-43).

Choi et al. further teach in the embodiment of figure 4B connecting the plurality of semiconducting nanotubes 100 with a single drain region 50 and a single source region 40.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a plurality of unit cells of the transistor in Choi et al.'s device, such that a plurality of semiconducting nanotubes are present in the device, and to connect the plurality of semiconducting nanotubes with a single drain region and a single source region, in order to use the device in a practical application which requires a plurality of semiconducting nanotubes, such as a nano sized transistor, and in order to simplify the processing steps of making the device and to simplify the operation of the device, respectively".

Choi et al. teach in the embodiment of figures 1-3 one unit cell (column 3, lines 41-43). Said unit cell comprises one nanotube 100, one drain region 50 and one source region 40. Choi et al. do not explicitly state in the embodiment of figures 1-3 that the final product to be used in a practical application comprises plurality of unit cells. However, it is well known in the art, that practical devices do not comprise only one transistor or one unit cell, but rather plurality of transistors or unit cells. Even appellants state in page 1, lines 9-10 of the specification that a chip, which is a practical device, comprises "many thousands to millions of FET's". It is further evident from Choi et al. that practical devices do not comprise one unit cell but plurality of unit cells.

Choi et al. recite in column 1, lines 29-38 the sizes of various practical semiconductor devices. It is unrealistic, and even impossible, that 1 Giga DRAM, for example, which occupies an area of approximately 0.32 microns square, will include only one transistor comprising one nanotube, one drain and one source.

Choi et al. further recites in column 1, lines 49-59 that *"In order to solve the aforementioned problems, it is a feature of an embodiment of the present invention to provide by vertical*

growth and selective deposition a vertical transistor ranging in size from several tens of nanometers to one micron using tera-bit scale carbon nanotubes as channels where each of the carbon nanotubes has a diameter of several nanometers and is grown on a nonconductive substrate having nano-sized holes. The lower and upper parts of each carbon nanotube are connected to a source and a drain, respectively, with a gate interposed between the source and the drain for performing switching".

It is evident from the above passage that Choi et al. explicitly state that a vertical transistor comprises plurality of carbon nanotubes wherein the lower and upper parts of each carbon nanotube are connected to a source and a drain, respectively.

Choi et al. further recites in column 1, line 63 to column 2, line 7, *that "In order to provide for these and other features of the present invention, there is provided a vertical nano-sized transistor using carbon nanotubes including an insulating layer preferably formed of one material selected from Al.sub.2 O.sub.3 and Si, the insulating layer having holes with nano-sized diameters; carbon nanotubes vertically aligned in the holes; gates formed over the insulating layer in the vicinity of the carbon nanotubes; a nonconductor film deposited on the gates to fill the holes; drains formed over the nonconductor film and the carbon nanotubes; and sources formed under the insulating layer and the carbon nanotubes. The sources and the drains are preferably formed of metal films".*

It is evident from the above passage that Choi et al. explicitly state that a vertical transistor comprises plurality of carbon nanotubes and plurality of source regions and drain regions.

Therefore, it is clear, or at least obvious, to form a practical device with industrial application which comprises plurality of unit cells or transistors.

Choi et al. further teach in the embodiment of figure 4B electrically coupling the plurality of semiconducting nanotubes 100 with a single drain region 50 and a single source region 40. The circuit diagram of figure 4B is depicted in figure 4A, wherein the

plurality of nanotubes 100 are electrically coupled and physically connected between one source region 40 and one drain region 50.

An artisan forming a practical device, based on the unit cell described in figures 1-3 of Choi et al., will form plurality of unit cells adjacent to each other, wherein each of the unit cells comprises one nanotube, one drain and one source. An artisan **will not** change the construction the unit cell depicted in figures 1-3. The final structure thus comprises plurality of unit cells formed adjacent to each other.

In order to simplify the processing steps of making the device and in order to simplify the operation of the device, the drain region of each respective unit cell will be connected to or connected as one drain line, and the source region of each respective unit cell will be connected to or connected as one source line, as taught in the embodiment of figures 4A and 4B of Choi et al., and as instructed by Choi et al. in column 1, lines 56-58. Clearly, it is easier to operate the device when external connections are formed only to one drain region and to one source region, instead of connecting the external connections to plurality of drain regions and plurality of source regions.

Thus, the modified final product of Choi et al. is identical to the structure, as recited in claim 1.

4. Appellants argue in the passage bridging pages 6 and 7 that "Appellant offers U.S. Patent No. 7,714,386 to Pesetskiet al. and entitled "Carbon Nanotube Field

Effect Transistor" as evidence of a patented industrial application that uses only a single nanotube".

4. Pesetskiet et al. describe a transistor or a unit cell comprising one nanotube, one drain and one source. Pesetskiet et al. does not describe an industrial practical device. Pesetskiet et al., however, recite in column 1, lines 10-50 industrial applications, such as linear amplifiers which are associated with pluralities of FET's transistors. As is well known in the art, and as stated by appellants in page 1, lines 9-10 of the specification, a chip, which is a practical device comprises "many thousands to millions of FET's".

5. Appellants argue on pages 7 and 8 that *"The statement made in Choi at column 3, lines 39-43 is inconsistent with all other statements found in Choi that regard the first embodiment shown in Figures 1-3".* Appellants interpret said statement by stating that *"At best, the disclosure in Choi is so unclear as to not support the Examiner's position that the ordinary meaning of these statements is that the final structure of each of the transistors includes "a plurality of carbon nanotubes". To the contrary and for reasons explained above, Appellant interprets the disclosure associated with Figures 1-3 of Choi to more reasonably mean that the device shown in Figures 1-3 operates as a transistor with its own source and drain independent of any other device of similar or identical construction in Choi. Choi does not state that the object shown in Figures 1-3 is a "unit cell" cannot be a transistor that includes one nanotube and that each of the identical "unit cells" cannot function as a discrete transistor".*

5. Appellants' interpretation of Choi et al.'s statement in column 3, lines 39-43 is inconsistent with Choi et al.'s description of the invention. As discussed above, Choi et al. explicitly recite in column 1, lines 49-59 and in column 1, line 63 to column 2, line 7 that Choi et al.'s final product comprises pluralities of nanotubes, drain regions and source regions. Therefore, Choi et al.'s statement in column 3, lines 39-43 is consistent with Choi et al.'s description of the invention when interpreted as describing the final product. The embodiment of figures 1-3, on the other, describes the construction of only one unit cell of the device. There is nothing unclear in Choi et al.'s disclosure, as argued by appellants.

6. Appellants argue on pages 9 and 10 that *"the Examiner characterizes the subject matter of claim 2 as a process limitation and disregards the claimed subject matter in his determination of patentability".* Appellants further argue that *"The Examiner fails to allege in the May 5, 2010 Office Action that the material disclosed in Choi for the source region (40) is composed of the claimed catalyst material and to support the allegation with statements from the written description of Choi".*

6. Claims 2 and 3 recite *"wherein said source [drain] is composed of a catalyst material effective for growing said at least one semiconducting nanotubes".*

The rejection recites that

"Regarding claims 2-3, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the source and drain of a catalyst material effective for growing said at least one semiconducting nanotube in Choi et al.'s device in order to simplify the processing steps of making the device.

Note that the process limitations of forming the source and drain of a catalyst material effective for growing said at least one semiconducting nanotube, would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced".

Thus, the Examiner did not disregard the claimed subject matter of claims 2 and 3. The examiner acknowledged that the material of the source or drain regions is a structural limitation by stating that "it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the source and drain of a catalyst material effective for growing said at least one semiconducting nanotube in Choi et al.'s device in order to simplify the processing steps of making the device". However, forming said at least one semiconducting nanotube by growth from a catalystic material is a process limitation.

Furthermore, Choi et al. recite in column 4, lines 21-25 that *"a carbon nanotube 100 is formed by vertically grown on the source 40".* Since Choi et al. teach growing said at least one semiconducting nanotube on the source region, then even if the source and/or drain region is not formed of a catalyst material, it would be obvious to form the source and drain regions of a catalyst material effective for growing said at least one semiconducting nanotube in order to simplify the processing steps of making the device by not using additional materials to grow the semiconducting nanotubes.

Please note that the processing steps of making the device is simplified by forming both the source and drain regions of the same material. In the alternative, it is conventional to reverse the polarity of the device. That is, the source region can serve as the drain region and vise versa. Appellants also states in page 11, lines 6-7 of the

specification that the source region can serve as the drain region and vise versa. In this case, the drain region would comprise the catalyst material, as claimed.

7. Summary:

Choi et al. teach the claimed limitations, as recited in claim 1, for the following three reasons:

1. Claim 1 recites, in part, a transistor device structure comprising: a source region, a drain region, a gate electrode positioned vertically between said source region and drain region, and *"a plurality of semiconducting nanotubes, each of said plurality of semiconducting nanotubes including a first end electrically coupled with said source region, a second end electrically coupled with said drain region".*

The limitation *"each of said plurality of semiconducting nanotubes including a first end electrically coupled with said source region, a second end electrically coupled with said drain region"* does not require physical contact between the nanotubes and the source and drain regions. The nanotubes are only required to make some electrical coupling with the source and drain regions. Furthermore, the electrical coupling can be made from any part of the nanotube, because each side of the nanotube can be considered as an "end" (please note ppellant does not claim that the first end is opposite to the second end). Since all the elements in one semiconductor device are electrically connected to each other, then a structure which comprises a source region, a drain region and a plurality of semiconducting nanotubes will read on the claimed structure.

Choi et al. clearly teach a semiconductor structure which comprises a source region, a drain region and a plurality of semiconducting nanotubes.

2. Although the broad recitation of the claim does not require physical contact between the nanotubes and the source and drain regions, the modified structure of Choi et al. teaches physical contact between the nanotubes and the source and drain regions (as discussed in section 3 above).

3. Choi et al. recite in column 1, lines 49-59 *"In order to solve the aforementioned problems, it is a feature of an embodiment of the present invention to provide by vertical growth and selective deposition* ***a vertical transistor*** *ranging in size from several tens of nanometers to one micron* ***using tera-bit scale carbon nanotubes as channels*** *where each of the carbon nanotubes has a diameter of several nanometers and is grown on a nonconductive substrate having nano-sized holes.* ***The lower and upper parts of each carbon nanotube are connected to a source and a drain, respectively, with a gate interposed between the source and the drain for performing switching"*** (emphasis added).

The above passage describes a structure which is not depicted in any of Choi et al.'s drawings, but is identical to the claimed structure. That is, the above passage recites, in part, a vertical transistor comprising nanotubes, wherein the lower and upper parts of each carbon nanotube are connected to a source region and a drain region, respectively, with a gate interposed between the source region and the drain region for performing switching. Claim 1 recites, in part, a transistor device structure comprising: a source region, a drain region, a gate electrode positioned vertically between said

source region and drain region, and *"a plurality of semiconducting nanotubes, each of said plurality of semiconducting nanotubes including a first end electrically coupled with said source region, a second end electrically coupled with said drain region".*

A claimed structure does not have to be depicted in a prior art reference in order to be rejected. Thus, although the structure described by Choi et al. in column 1, lines 49-59 is not depicted in any of the drawings, this structure is identical to the claimed structure.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

O.N.

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